FIG. 1

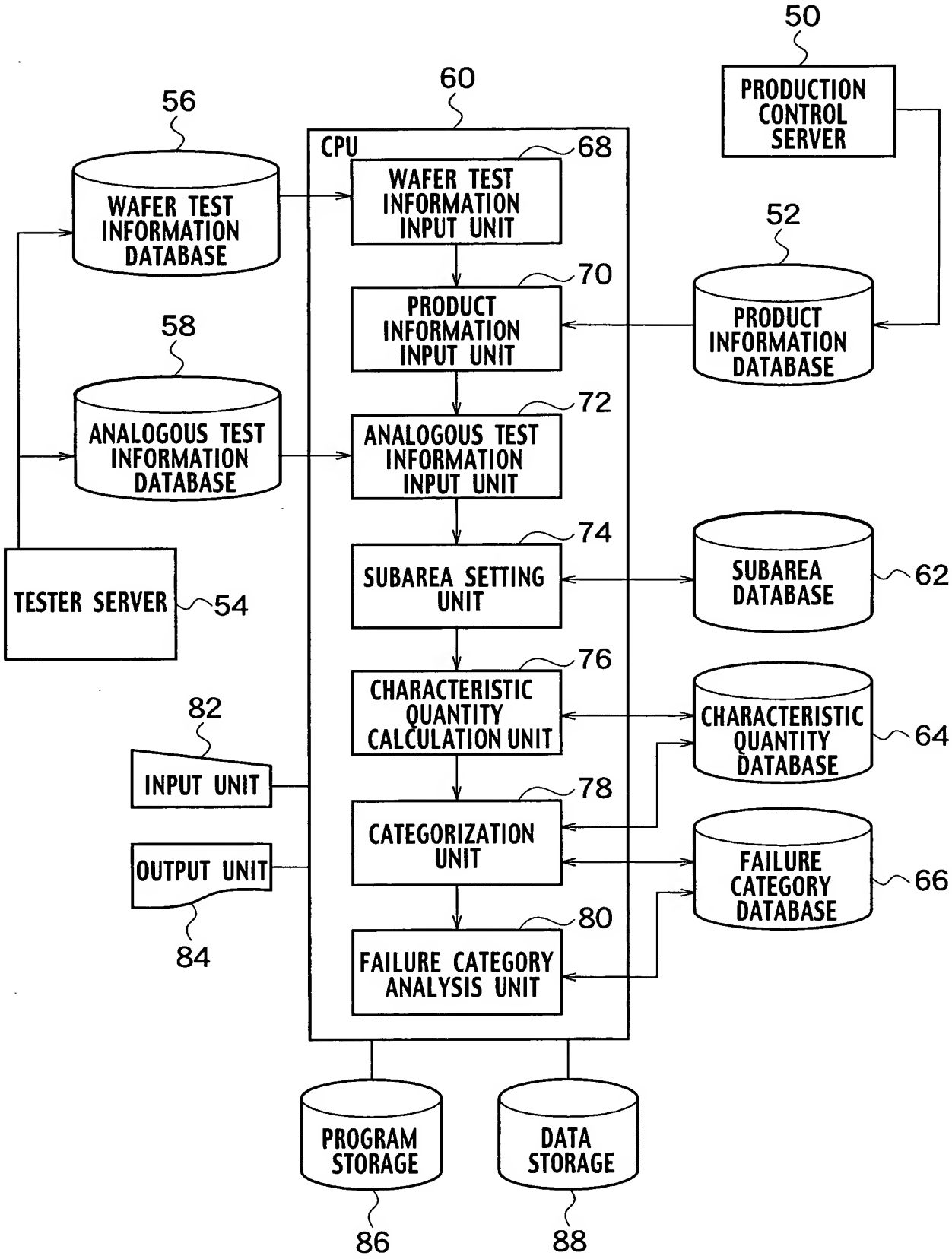

50
PRODUCTION CONTROL SERVER
60
CPU
56
WAFER TEST INFORMATION DATABASE
68
WAFER TEST INFORMATION INPUT UNIT
52
70
PRODUCT INFORMATION INPUT UNIT
PRODUCT INFORMATION DATABASE
58
ANALOGOUS TEST INFORMATION DATABASE
72
ANALOGOUS TEST INFORMATION INPUT UNIT
74
SUBAREA SETTING UNIT
SUBAREA DATABASE
62
TESTER SERVER
54
76
CHARACTERISTIC QUANTITY CALCULATION UNIT
CHARACTERISTIC QUANTITY DATABASE
64
82
INPUT UNIT
78
CATEGORIZATION UNIT
OUTPUT UNIT
FAILURE CATEGORY DATABASE
66
80
84
FAILURE CATEGORY ANALYSIS UNIT
PROGRAM STORAGE
DATA STORAGE
86
88

FIG. 2

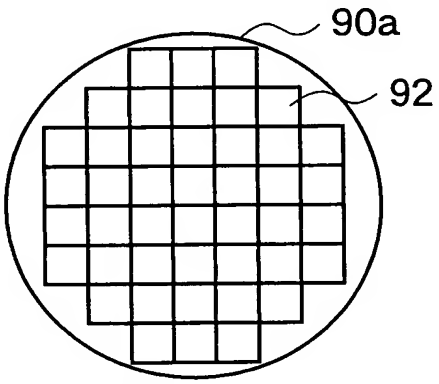
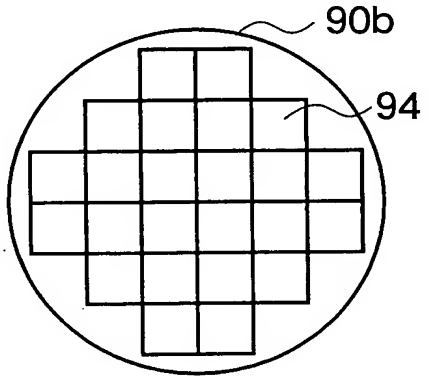
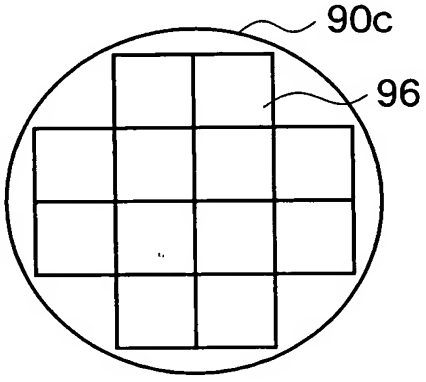
PRODUCT NAME	PRODUCT	CHIP LAYOUT
PRODUCT A	MEMORY	
PRODUCT B	LOGIC	
PRODUCT C	MEMORY MERGED LOGIC	

FIG. 3

PRODUCT A		PRODUCT B		PRODUCT C	
ELECTRIC TEST	FAILURE CODE	ELECTRIC TEST	FAILURE CODE	ELECTRIC TEST	FAILURE CODE
DC	DC	POWER SHORT	PS	DC	DC
FUNCTION	FC	FUNCTION	FC	AD / DA1	A1
MARGIN	MA	FREQUENCY	FQ	AD / DA2	A2
		OTHER LOGIC	OL		

FIG. 4

ANALOGOUS ELECTRIC TEST 1			ANALOGOUS ELECTRIC TEST 2			ANALOGOUS ELECTRIC TEST 3		
PRODUCT	ELECTRIC TEST	FAILURE CODE	PRODUCT	ELECTRIC TEST	FAILURE CODE	PRODUCT	ELECTRIC TEST	FAILURE CODE
PRODUCT A	DC	DC	PRODUCT A	FUNCTION	FC	PRODUCT A	MARGIN	MA
PRODUCT B	POWER SHORT	PS	PRODUCT B	FUNCTION	FC	PRODUCT B	FREQUENCY	FQ
PRODUCT C	DC	DC	PRODUCT C	OTHER LOGIC	OL	PRODUCT C	AD / DA2	A2
			PRODUCT D	AD / DA1	A1			

FIG. 5

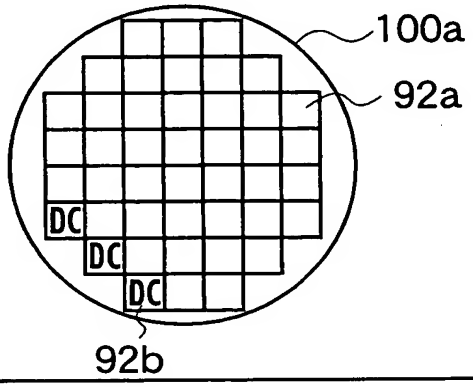
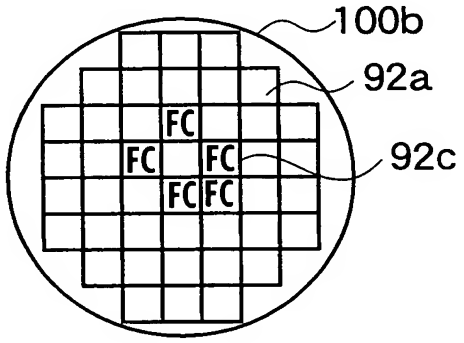
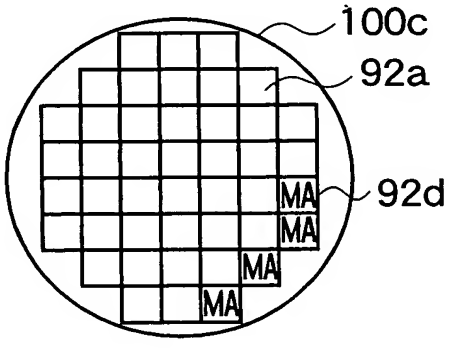
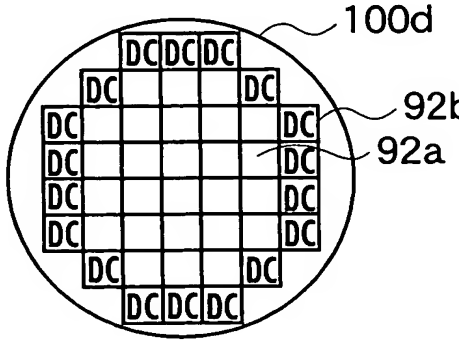
PRODUCT A WAFER NUMBER	ELECTRIC TEST RESULT
1	
2	
3	
4	

FIG. 6

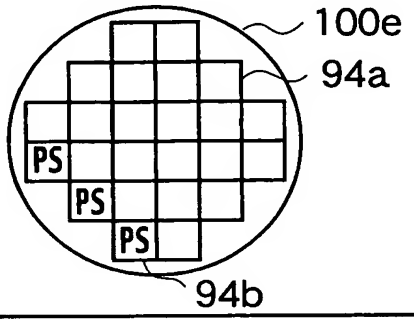
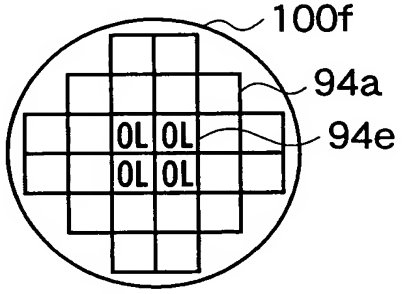
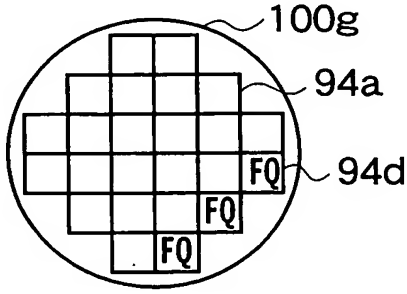
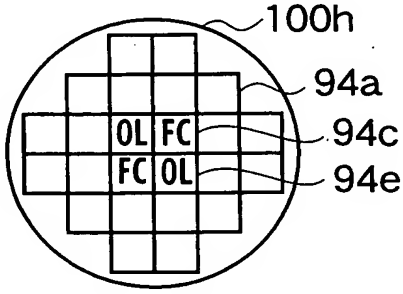
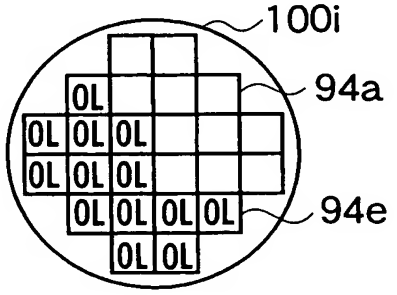
PRODUCT B WAFER NUMBER	ELECTRIC TEST RESULT
5	
6	
7	
8	
9	

FIG. 7

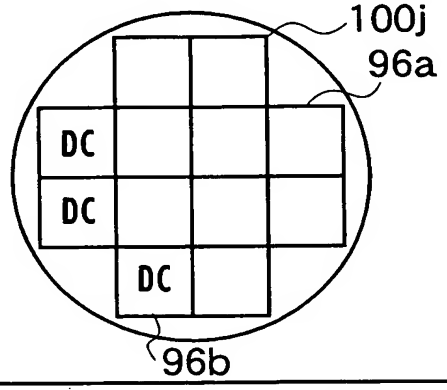
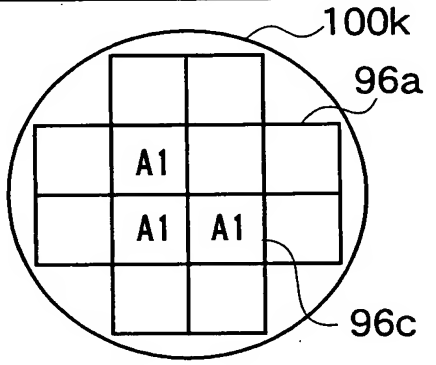
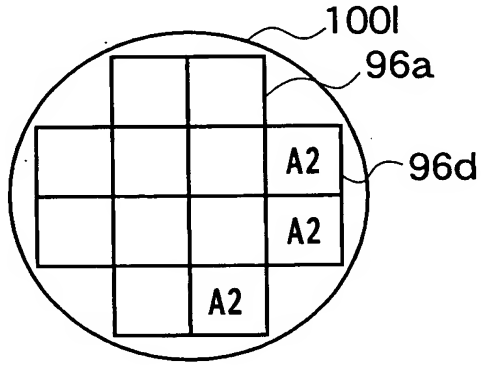
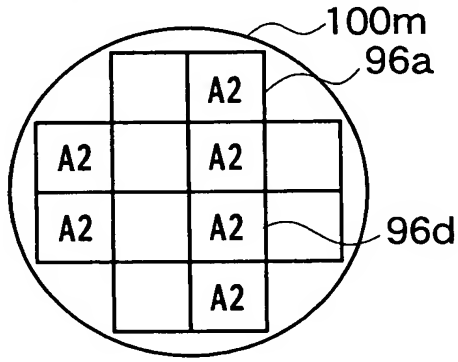
PRODUCT C WAFER NUMBER	ELECTRIC TEST RESULT
10	
11	
12	
13	

FIG. 8

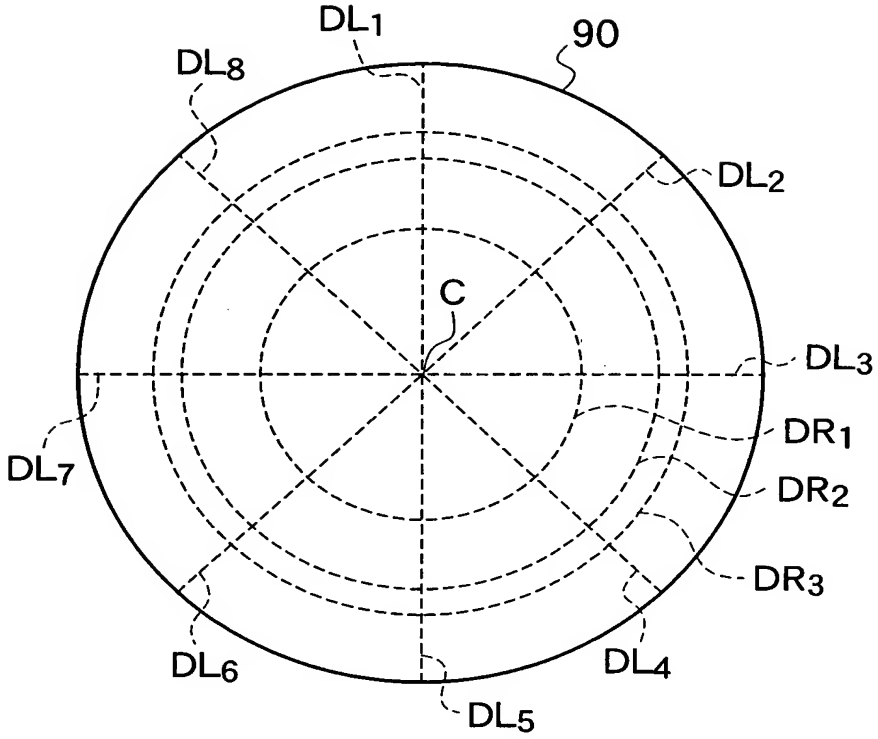


FIG. 9

AREA NUMBER	SUBAREA
1	[DR_3OUTSIDE] V [DL_3-DL_4-DL_5-DL_6-DL_7]
2	[DR_3OUTSIDE] V [DL_7-DL_8-DL_1-DL_2-DL_3]
3	[DR_2OUTSIDE] V [DL_8-DL_1-DL_2-DL_3-DL_4]
⋮	⋮
76	[DR_2INSIDE] V [DL_3-DL_4-DL_5]
⋮	⋮
150	[DR_1INSIDE] V [DL_4-DL_5-DL_6-DL_7-DL_8]

FIG. 10

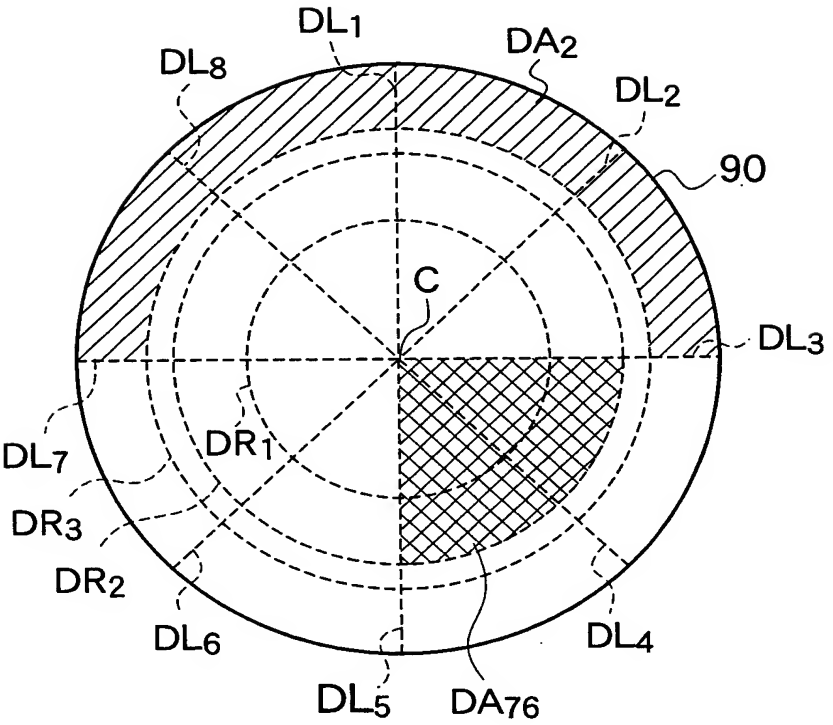

DL1
DA2
DL8
DL2
90
C
DL3
DR1
DL7
DR3
DR2
DL6
DL4
DL5
DA76

FIG. 11

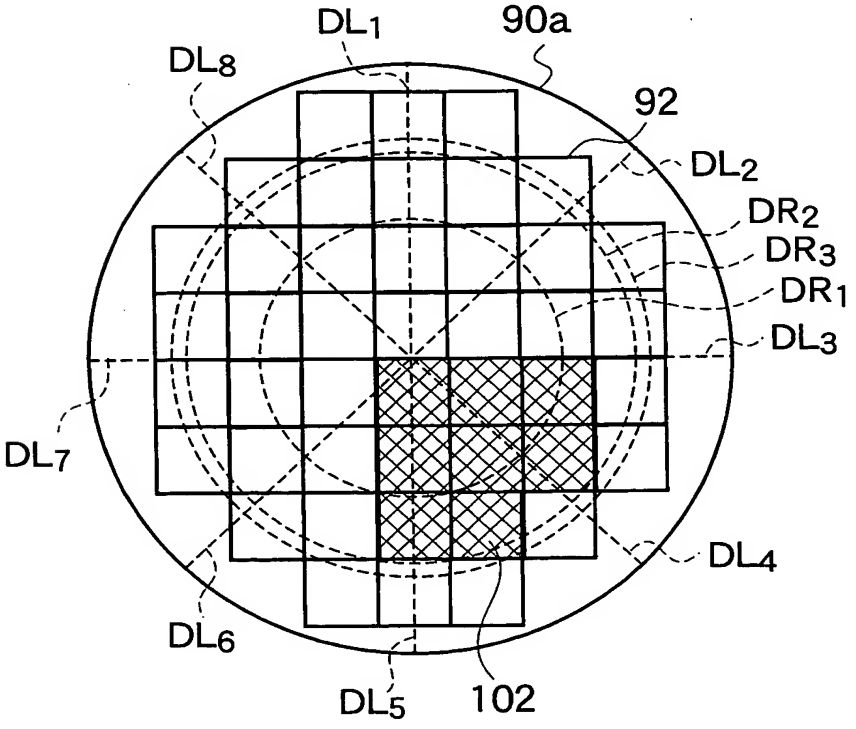

DL1
90a
DL8
92
DL2
DR2
DR3
DR1
DL3
DL7
DL4
DL6
DL5
102

FIG. 12

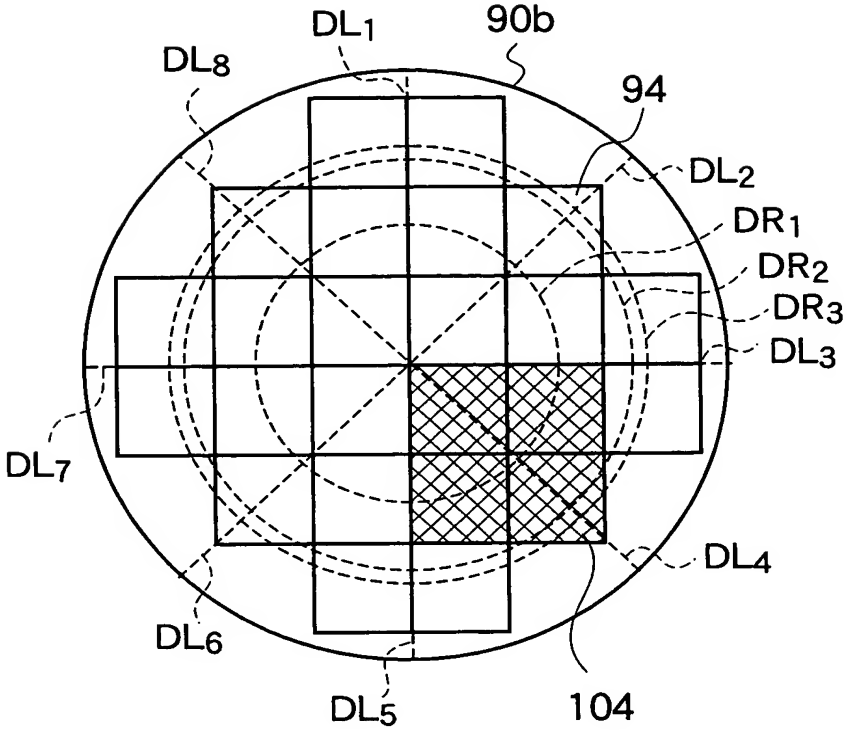

DL1
90b
DL8
94
DL2
DR1
DR2
DR3
DL3
DL7
DL4
DL6
DL5
104

FIG. 13

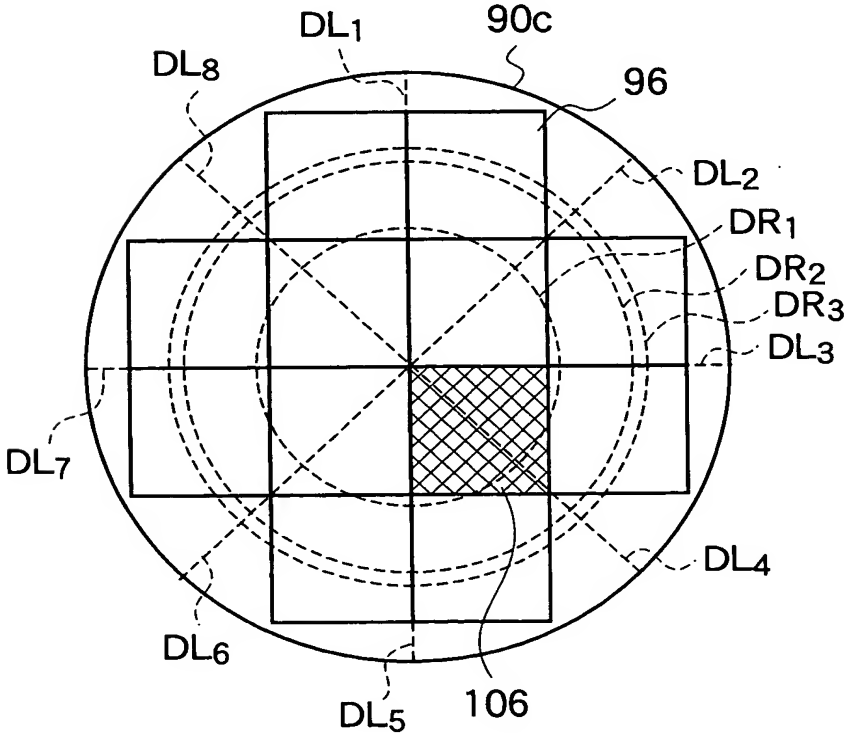

DL1
90c
DL8
96
DL2
DR1
DR2
DR3
DL3
DL7
DL4
DL6
DL5
106

FIG. 14

PRODUCT A					
ELECTRIC TEST	AREA NUMBER	WAFER NUMBER			
		1	2	3	4
DC	1	0.3	0	0.01	0.32
	2	0.5	0	0	0.12
	3	0.2	0.01	0	0.05
	⋮	⋮	⋮	⋮	⋮
	150	0.5	0	0	0.32
FUNCTION	1	0	0.67	0	0
	2	0	0.23	0.02	0
	3	0.01	0.15	0	0.01
	⋮	⋮	⋮	⋮	⋮
	150	0	0.42	0	0
MARGIN	1	0	0	0.2	0.01
	2	0	0.01	0.1	0
	3	0	0	0.03	0
	⋮	⋮	⋮	⋮	⋮
	150	0.02	0	0.12	0

FIG. 15

ANALOGOUS ELECTRIC TEST	PRODUCT A , WAFER No.1			PRODUCT B , WAFER No.5		
	ELECTRIC TEST	AREA NUMBER	FAILURE DENSITY	ELECTRIC TEST	AREA NUMBER	FAILURE DENSITY
ANALOGOUS ELECTRIC TEST 1	DC FAILURE	1	0.3	POWER SHORT FAILURE	1	0.28
		2	0.5		2	0.43
		3	0.2		3	0.1
		⋮	⋮		⋮	⋮
		150	0.5		150	0.67
ANALOGOUS ELECTRIC TEST 2	FUNCTION FAILURE	1	0	FUNCTION FAILURE + OTHER LOGIC FAILURE	1	0
		2	0		2	0.01
		3	0.01		3	0
		⋮	⋮		⋮	⋮
		150	0		150	0
ANALOGOUS ELECTRIC TEST 3	MARGIN FAILURE	1	0	FREQUENCY FAILURE	1	0
		2	0		2	0.01
		3	0		3	0
		⋮	⋮		⋮	⋮
		150	0.02		150	0

FIG. 16

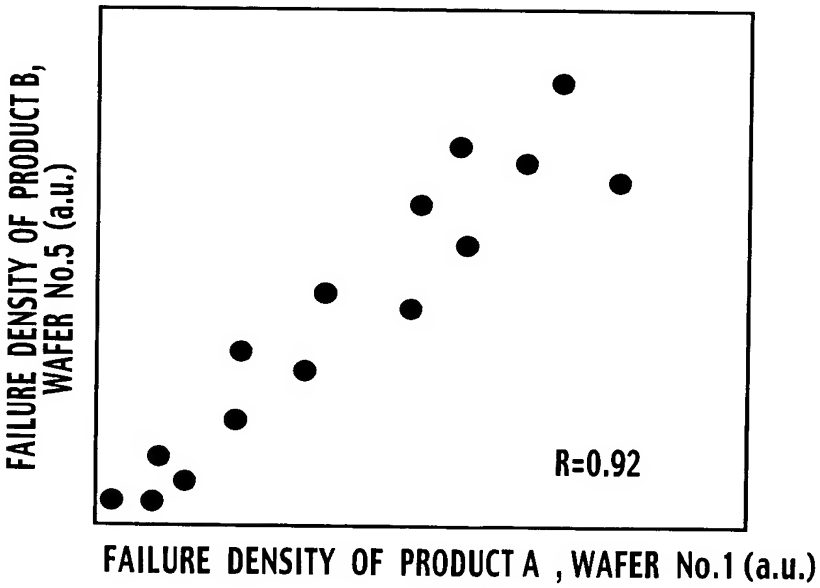


FIG. 17

		PRODUCT A	PRODUCT A	PRODUCT A	PRODUCT A	PRODUCT B		PRODUCT C		PRODUCT C
		WAFER No.1	WAFER No.2	WAFER No.3	WAFER No.4	WAFER No.5		WAFER No.10		WAFER No.13
PRODUCT A	WAFER No.1	1	0.01	0.12	0.08	0.92		0.91		0.01
PRODUCT A	WAFER No.2	0.01	1	0.03	0.09	0.08	.....	0.01	.....	0.01
PRODUCT A	WAFER No.3	0.12	0.03	1	0.12	0.01		0.09		0.01
PRODUCT A	WAFER No.4	0.08	0.09	0.12	1	0.23		0.01		0.02
PRODUCT B	WAFER No.5	0.92	0.08	0.01	0.23	1		0.87		0.09
		⋮						⋮		⋮
PRODUCT C	WAFER No.10	0.91	0.01	0.09	0.01	0.87	.....	1	.....	0.07
		⋮						⋮		⋮
PRODUCT C	WAFER No.13	0.01	0.01	0.01	0.02	0.09	.....	0.07	.....	1

FIG. 18

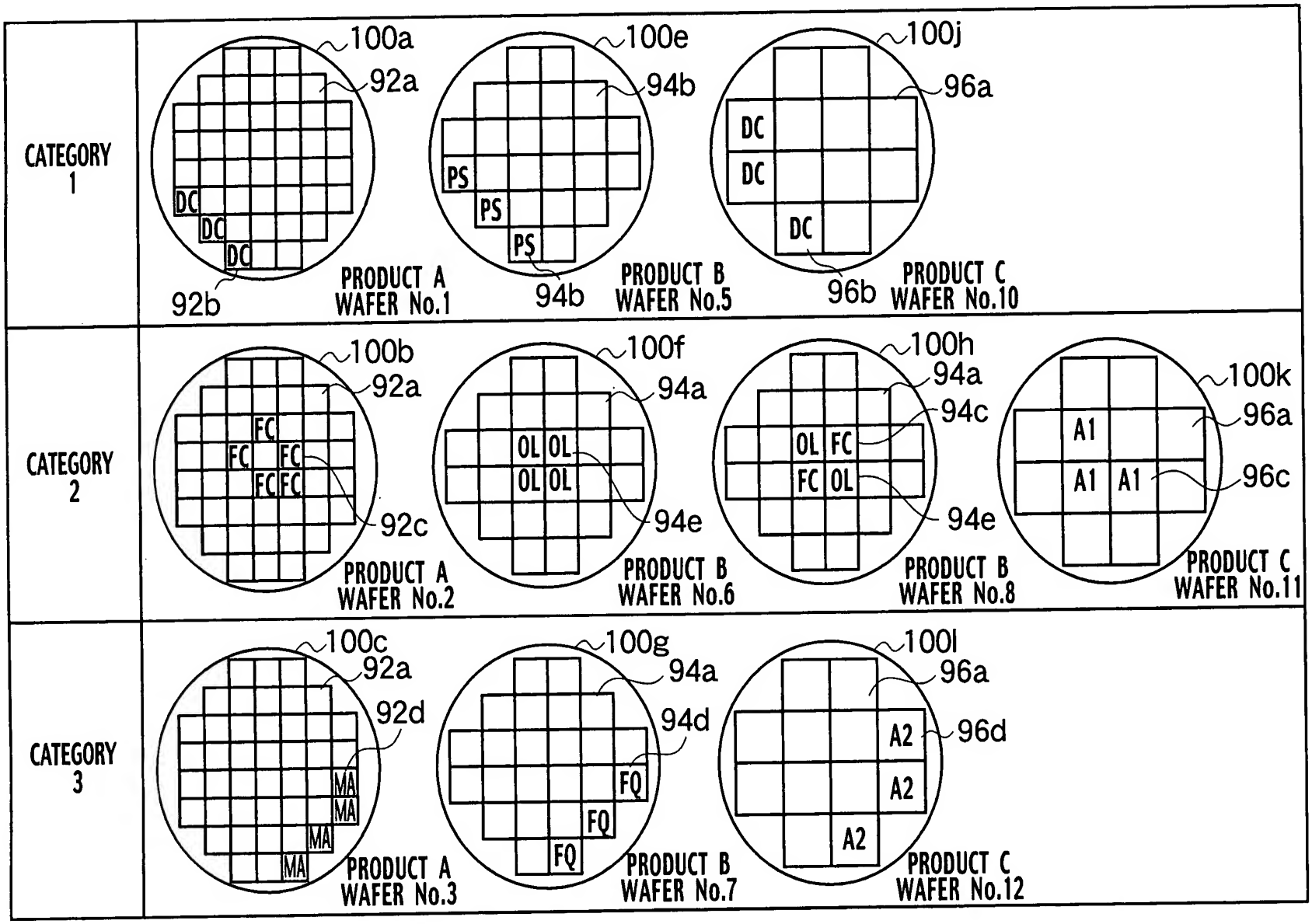

CATEGORY 1
100a
92a
DC
DC
DC
92b
PRODUCT A WAFER No.1
100e
94b
PS
PS
PS
94b
PRODUCT B WAFER No.5
100j
96a
DC
DC
DC
96b
PRODUCT C WAFER No.10
CATEGORY 2
100b
92a
FC
FC
FC
FC
FC
92c
PRODUCT A WAFER No.2
100f
94a
OL OL
OL OL
94e
PRODUCT B WAFER No.6
100h
94a
94c
OL FC
FC OL
94e
PRODUCT B WAFER No.8
100k
96a
A1
A1 A1
96c
PRODUCT C WAFER No.11
CATEGORY 3
100c
92a
92d
MA
MA
MA
MA
PRODUCT A WAFER No.3
100g
94a
94d
FQ
FQ
FQ
PRODUCT B WAFER No.7
100l
96a
A2
A2
A2
96d
PRODUCT C WAFER No.12

FIG. 19

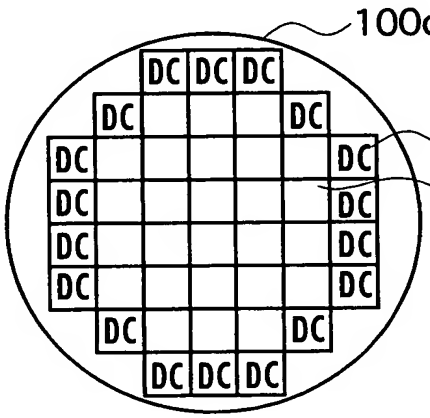
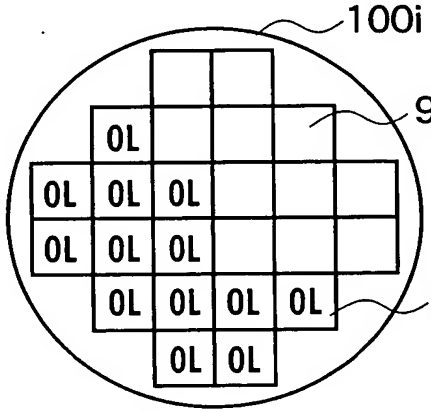
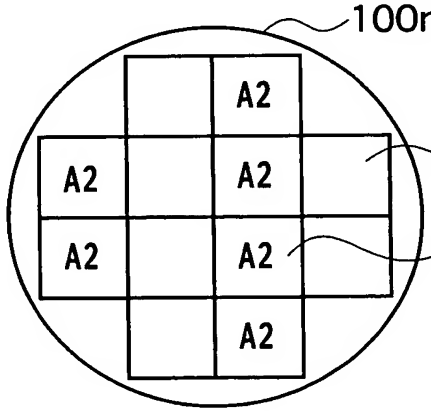
CATEGORY 4	
CATEGORY 5	
CATEGORY 6	

FIG. 20

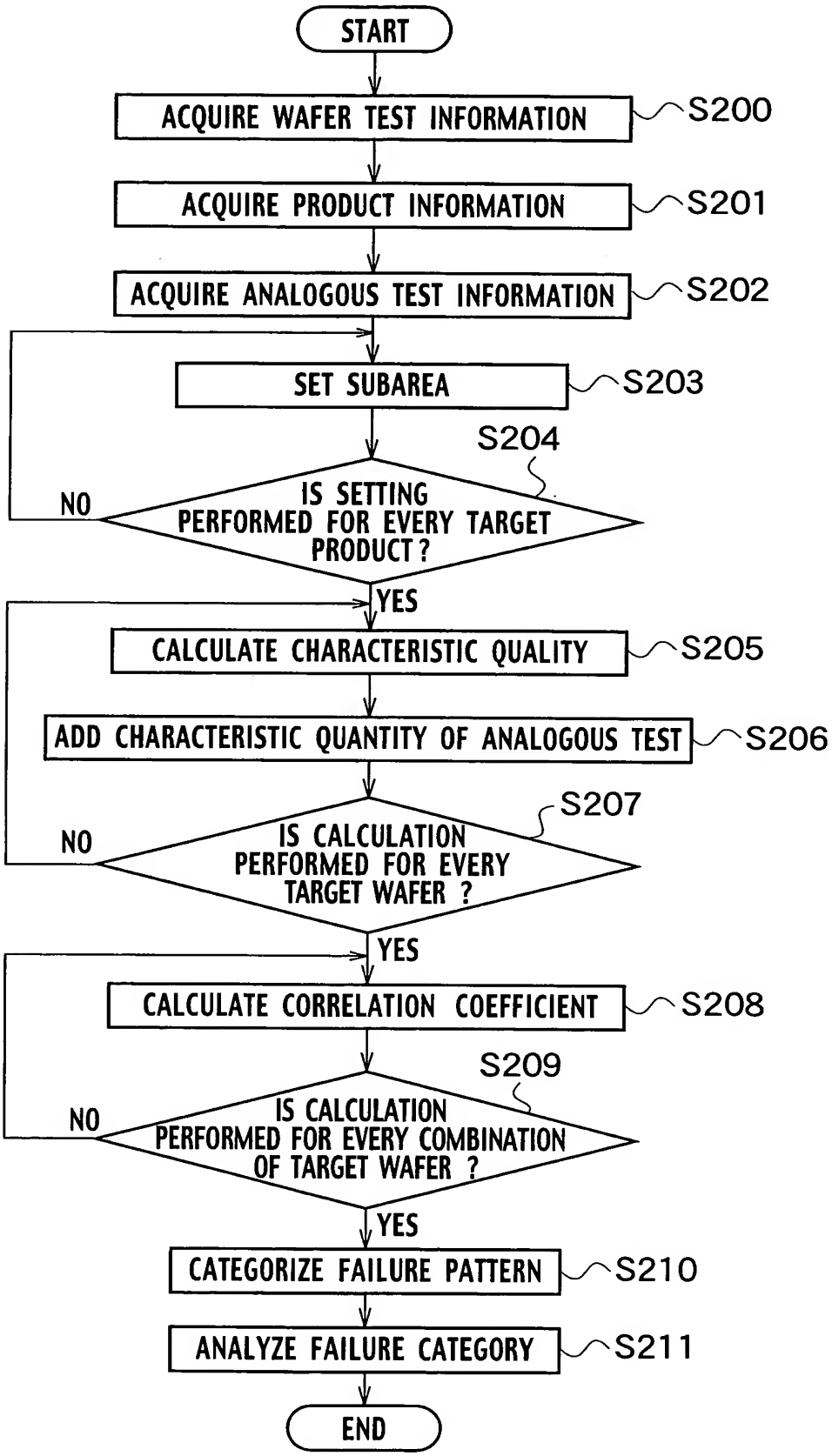

START
ACQUIRE WAFER TEST INFORMATION
S200
ACQUIRE PRODUCT INFORMATION
S201
ACQUIRE ANALOGOUS TEST INFORMATION
S202
SET SUBAREA
S203
S204
IS SETTING PERFORMED FOR EVERY TARGET PRODUCT?
NO
YES
CALCULATE CHARACTERISTIC QUALITY
S205
ADD CHARACTERISTIC QUANTITY OF ANALOGOUS TEST
S206
S207
IS CALCULATION PERFORMED FOR EVERY TARGET WAFER ?
NO
YES
CALCULATE CORRELATION COEFFICIENT
S208
S209
IS CALCULATION PERFORMED FOR EVERY COMBINATION OF TARGET WAFER ?
NO
YES
CATEGORIZE FAILURE PATTERN
S210
ANALYZE FAILURE CATEGORY
S211
END

FIG. 21

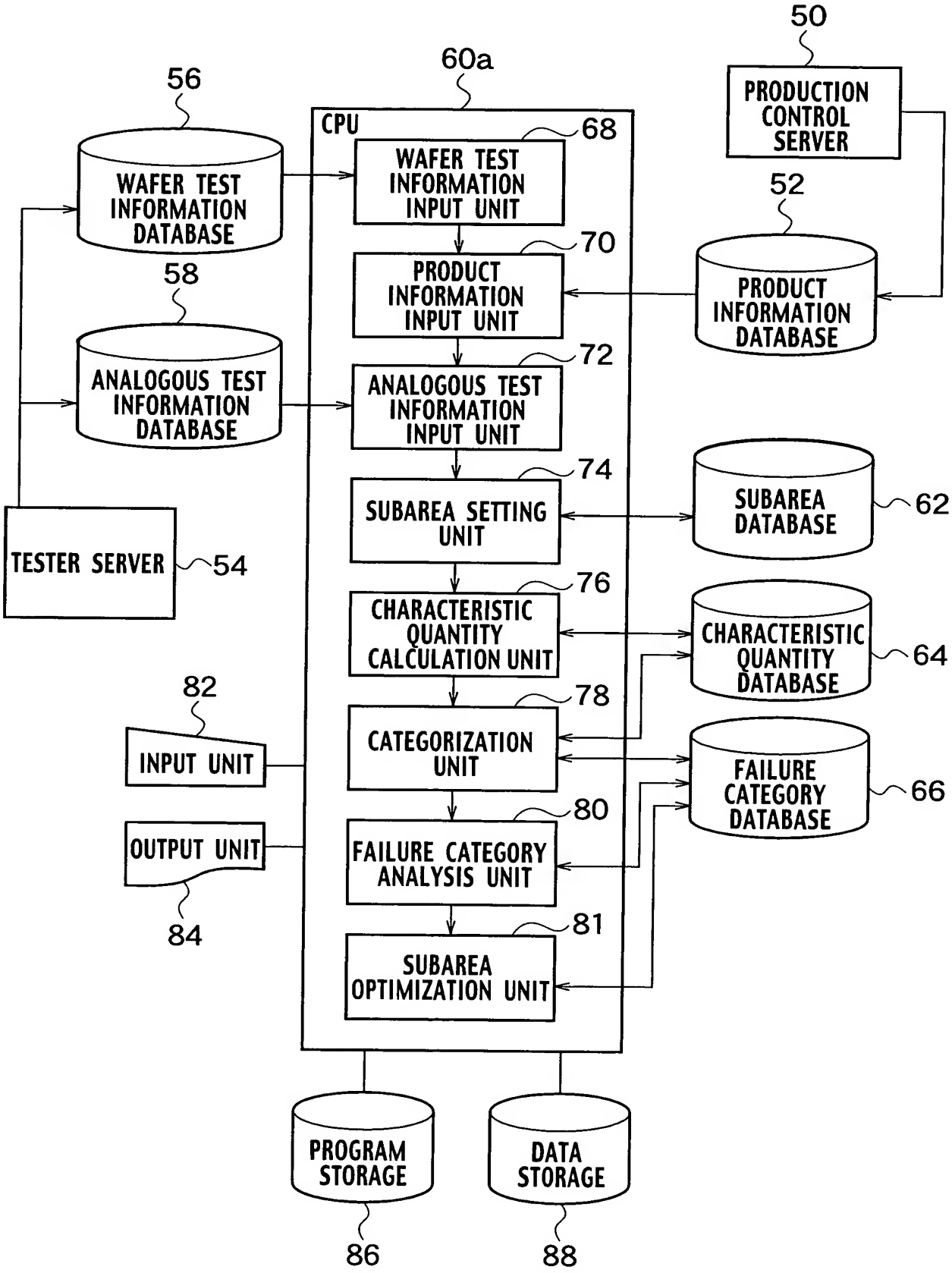

50
60a
56
CPU
68
PRODUCTION CONTROL SERVER
WAFER TEST INFORMATION DATABASE
WAFER TEST INFORMATION INPUT UNIT
52
70
PRODUCT INFORMATION INPUT UNIT
PRODUCT INFORMATION DATABASE
58
ANALOGOUS TEST INFORMATION DATABASE
72
ANALOGOUS TEST INFORMATION INPUT UNIT
74
SUBAREA SETTING UNIT
SUBAREA DATABASE
62
TESTER SERVER
54
76
CHARACTERISTIC QUANTITY CALCULATION UNIT
CHARACTERISTIC QUANTITY DATABASE
64
82
78
INPUT UNIT
CATEGORIZATION UNIT
FAILURE CATEGORY DATABASE
66
80
OUTPUT UNIT
FAILURE CATEGORY ANALYSIS UNIT
84
81
SUBAREA OPTIMIZATION UNIT
PROGRAM STORAGE
DATA STORAGE
86
88

FIG. 22

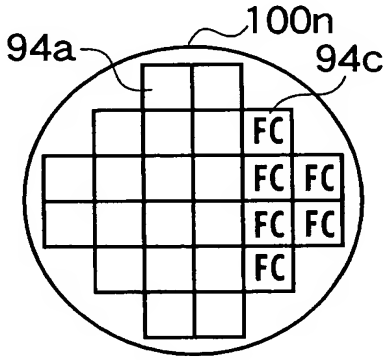
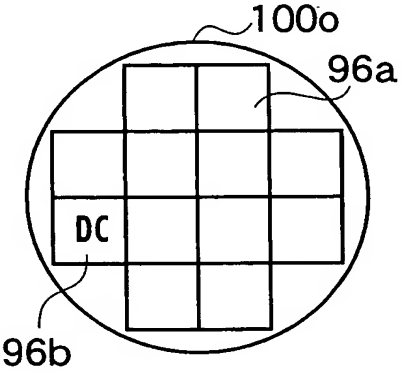
	PASS / FAIL MAP	ABNORMAL PROCESS NUMBER	ABNORMAL MANUFACTURING APPRATUS	TEST STATISTIC
CATEGORY 7		136	M1	13.6
CATEGORY 8		96	P1	12.7

FIG. 23

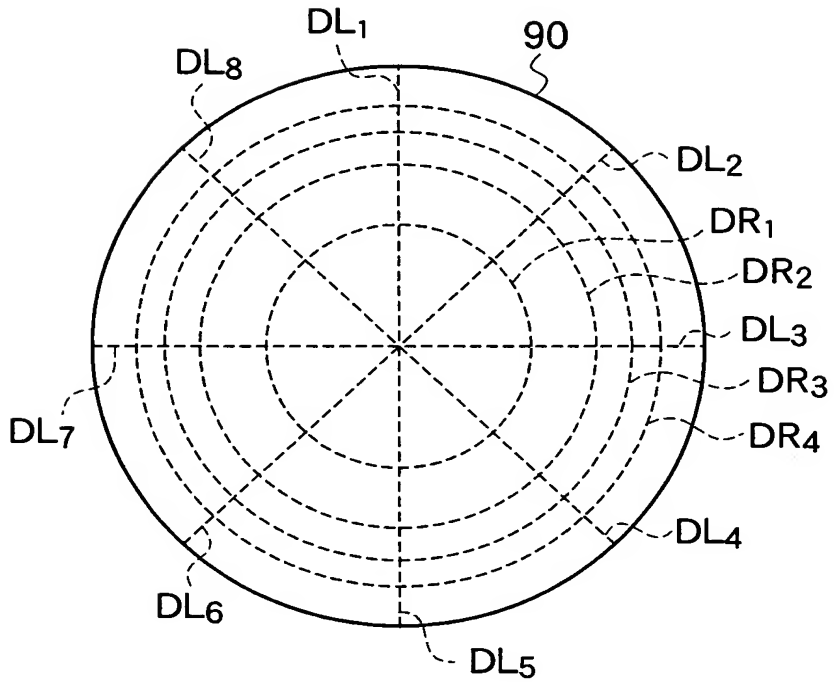

DL1
90
DL8
DL2
DR1
DR2
DL3
DR3
DL7
DR4
DL4
DL6
DL5

FIG. 24

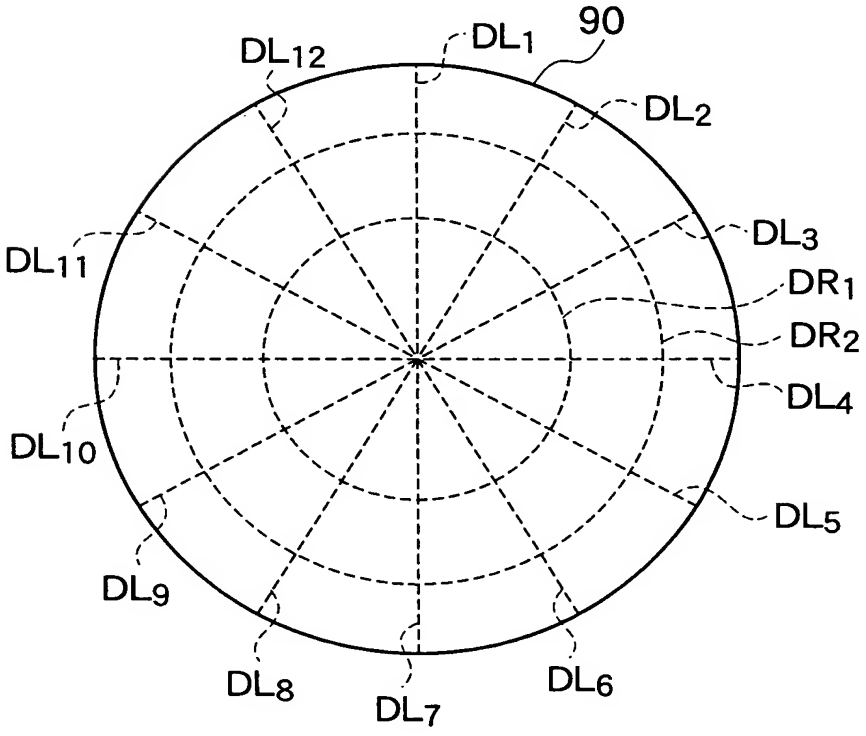

90
DL1
DL12
DL2
DL3
DL11
DR1
DR2
DL4
DL10
DL5
DL9
DL8
DL7
DL6

FIG. 25

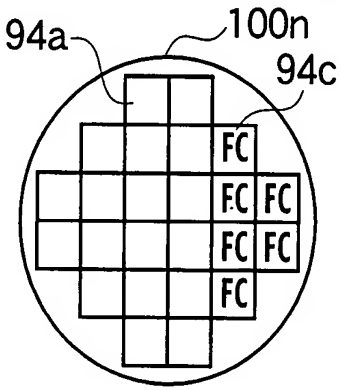
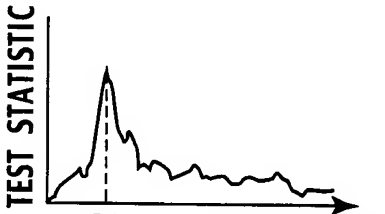
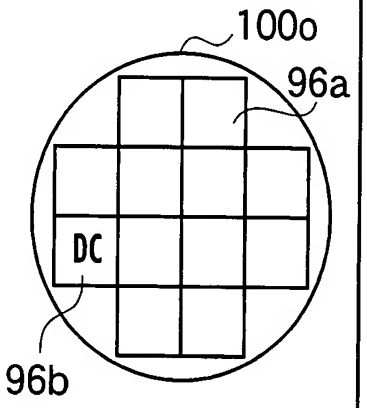
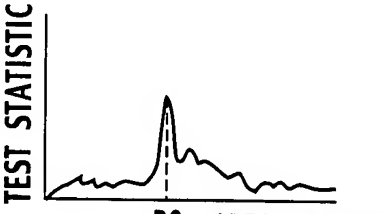
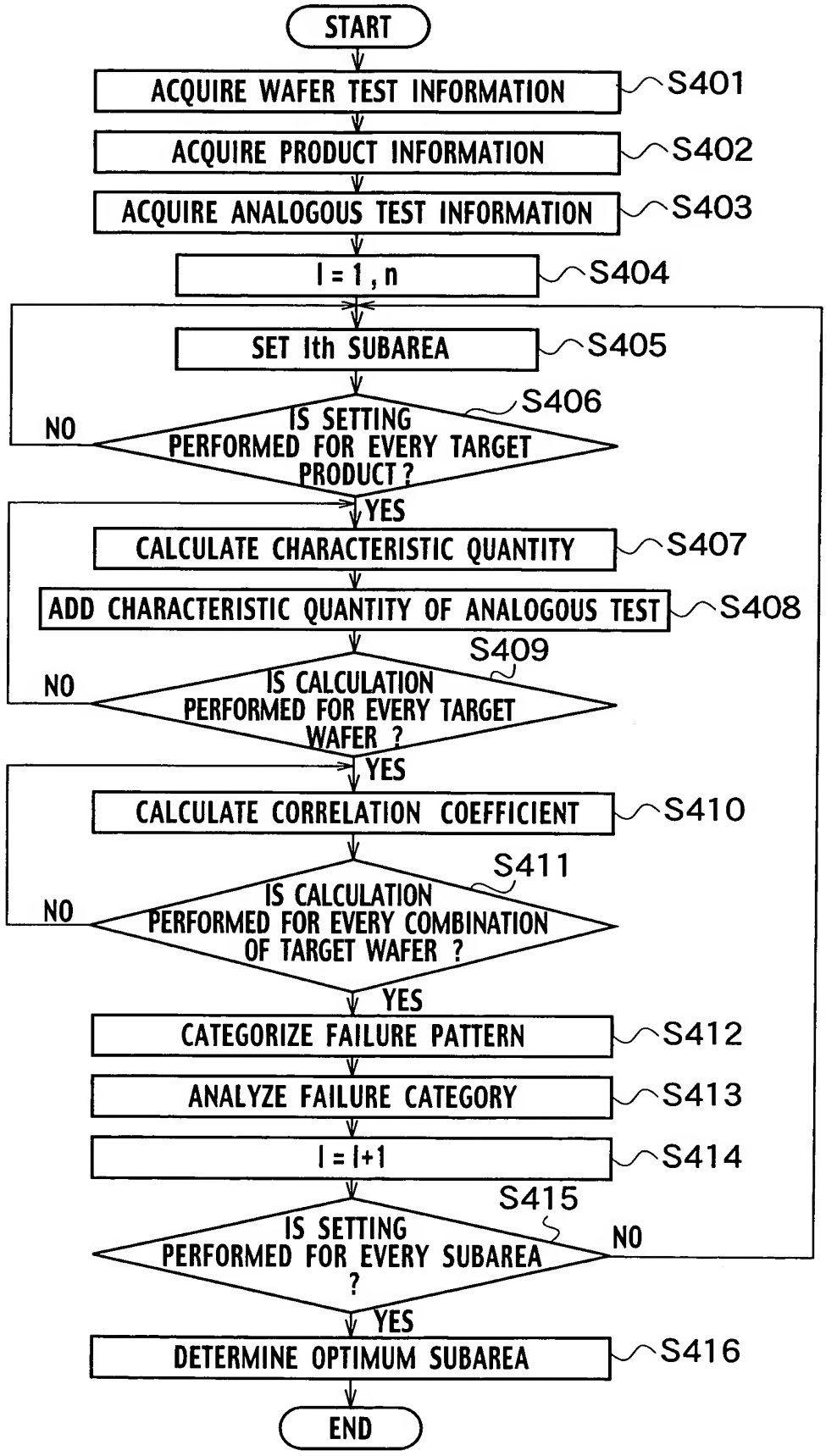
	PASS / FAIL MAP	VARIATION OF TEST STATISTIC	ABNORMAL PROCESS NUMBER	ABNORMAL MANUFACTURING APPARATUS	TEST STATISTIC
CATEGORY 7		 D1 : DIVIDING CIRCLE : 2 DIVIDING LINE : 5	136	M1	27.6
CATEGORY 8		 D2 : DIVIDING CIRCLE : 6 DIVIDING LINE : 12	82	P2	24.3

FIG. 26


START
ACQUIRE WAFER TEST INFORMATION
S401
ACQUIRE PRODUCT INFORMATION
S402
ACQUIRE ANALOGOUS TEST INFORMATION
S403
I = 1 , n
S404
SET Ith SUBAREA
S405
S406
IS SETTING PERFORMED FOR EVERY TARGET PRODUCT ?
NO
YES
CALCULATE CHARACTERISTIC QUANTITY
S407
ADD CHARACTERISTIC QUANTITY OF ANALOGOUS TEST
S408
S409
IS CALCULATION PERFORMED FOR EVERY TARGET WAFER ?
NO
YES
CALCULATE CORRELATION COEFFICIENT
S410
S411
IS CALCULATION PERFORMED FOR EVERY COMBINATION OF TARGET WAFER ?
NO
YES
CATEGORIZE FAILURE PATTERN
S412
ANALYZE FAILURE CATEGORY
S413
I = I+1
S414
S415
IS SETTING PERFORMED FOR EVERY SUBAREA ?
NO
YES
DETERMINE OPTIMUM SUBAREA
S416
END